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processors like the Intel 80286 and Motorola 68020, some additional design features were used: Conditional execution of most instructions reduces branch overhead and compensates for the lack of a branch predictor in early chips. Arithmetic instructions reduce condition codes only when desired. 32-bit barrel shifter can be used without performance penalty with most arithmetic instructions and address calculations. Has powerful indexed addressing modes. A link register supports fast leaf function calls. A simple, but fast, 2-priority-level interrupt subsystem has switched register banks. ARM includes integer arithmetic operations for add, subtract, and multiply; some versions of the architecture also support divide operations. ARM supports 32-bit × 32-bit multiplies with either a 32-bit result or 64-bit result, though Cortex-M0 / M0+ / M1 cores do not support 64-bit results.[112] Some ARM cores also support 16-bit × 16-bit and 32-bit × 16-bit multiplies. The divide instructions are only included in the following ARM architectures: Armv7-M and Armv7E-M architectures always include divide instructions.[113] Armv7-R architecture always includes divide instructions in the Thumb instruction set, but optionally in its 32-bit instruction set.[114] Armv7-A architecture optionally includes the divide instructions. The instructions might not be implemented, or implemented only in the Thumb instruction set, or implemented in both the Thumb and ARM instruction sets, or implemented if the Virtualization Extensions are included.[114] Registers across CPU modes usr sys svc abt und irq fiq R0 R1 R2 R3 R4 R5 R6 R7 R8 R8 fiq R9 R9 fiq R10 R10 fiq R11 R11 fiq R12 R12 fiq R13 R13 svc R13 abt R13 und R13 irq R13 fiq R14 R14 svc R14 abt R14 und R14 irq R14 fiq R15 CPSR SPSR_svc SPSR_abt SPSR und SPSR_irq SPSR_fiq Registers R0 through R7 are the same across all CPU modes; they are never banked. Registers R8 through R12 are the same across all CPU modes except FIQ mode. FIQ mode has its own distinct R8 through R12 registers. R13 and R14 are banked across all privileged CPU modes except system mode. That is, each mode that can be entered because of an exception has its own R13 and R14. These registers generally contain the stack pointer and the return address from function calls, respectively. Aliases: R13 is also referred to as SP, the stack pointer. R14 is also referred to as LR, the link register. R15 is also referred to as PC, the program counter. The Current Program Status Register (CPSR) has the following 32 bits.[115] M (bits 0–4) is the processor mode bits. T (bit 5) is the Thumb state bit. F (bit 6) is the FIQ disable bit. I (bit 7) is the IRQ disable bit. A (bit 8) is the imprecise data abort disable bit. E (bit 9) is the data endianness bit. IT (bits 10–15 and 25–26) is the if-then state bits. GE (bits 16–19) is the greater-than-or-equal-to bits. DNM (bits 20–23) is the do not modify bits. J (bit 24) is the Java state bit. Q (bit 27) is the sticky overflow bit. V (bit 28) is the overflow bit. C (bit 29) is the carry/borrow/extend bit. Z (bit 30) is the zero bit. N (bit 31) is the negative/less than bit. Almost every ARM instruction has a conditional execution feature called predication, which is implemented with a 4-bit condition code selector (the predicate). To allow for unconditional execution, one of the four-bit codes causes the instruction to be always executed. Most other CPU architectures only have condition codes on branch instructions.[116] Though the predicate takes up four of the 32 bits in an instruction code, and thus cuts down significantly on the encoding bits available for displacements in memory access instructions, it avoids branch instructions when generating code for small if statements. Apart from eliminating the branch instructions themselves, this preserves the fetch/decode/execute pipeline at the cost of only one cycle per skipped instruction. An algorithm that provides a good example of conditional execution is the subtraction-based Euclidean algorithm for computing the greatest common divisor. In the C programming language, the algorithm can be written as: int gcd(int a, int b) { while (a != b) // We enter the loop when a < b or a > b, but not when a == b if (a > b) // When a > b we do this a -= b; else // When a < b we do that (no "if (a < b)" needed since a != b is checked in while condition) b -= a; return a; } The same algorithm can be rewritten in a way closer to target ARM instructions as: loop: // Compare a and b GT = a > b; LT = a < b; NE = a != b; // Perform operations based on flag results if (GT) a -= b; // Subtract *only* if greater-than if (LT) b -= a; // Subtract *only* if less-than if (NE) goto loop; // Loop *only* if compared values were not equal return a; and coded in assembly language as: ; assign a to register r0, b to r1 loop: CMP r0, r1 ; set condition "NE" if (a ≠ b), ; "GT" if (a > b), ; or "LT" if (a < b) SUBGT r0, r0, r1 ; if "GT" (Greater Than), then a = a - b SUBLT r1, r1, r0 ; if "LT" (Less Than), then b = b - a BNE loop ; if "NE" (Not Equal), then loop B lr ; return which avoids the branches around the then and else clauses. If r0 and r1 are equal then neither of the SUB instructions will be executed, eliminating the need for a conditional branch to implement the while check at the top of the loop, for example had SUBLE (less than or equal) been used. One of the ways that Thumb code provides a more dense encoding is to remove the four-bit selector from non-branch instructions. Another feature of the instruction set is the ability to fold shifts and rotates into the data processing (arithmetic, logical, and register-register move) instructions, so that, for example, the statement in C language: a += 0